



28th IEEE European Test Symposium 2023  
May, Monday 22 to Friday 26 in Venice, Italy  
[CAS.POLITO.IT/ETS23](https://cas.polito.it/ets23)



## *ETS23 - Preliminary Program*



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## MONDAY, MAY 22ND, 2023

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### TSS Tutorials at ETS23

15:00 – 19:00

*TSS Tutorials are free of charge for ETS23 attendees*

#### Auditorium

Tutorial 1 : Machine Learning in Logic Circuit

Diagnosis: Haralampos

MODERATOR : TO BE ANNOUNCED

**PRESENTER : SHAWN BLANTON - CARNEGIE MELLON UNIVERSITY, US**

Abstract : In this seminar, we examine representative work of the use of ML in diagnosis from the Advanced Chip Testing Laboratory of Carnegie Mellon University. We partition the work into three categories, namely, pre-diagnosis, during-diagnosis, and post-diagnosis. Pre-diagnosis is concerned with any activities that are performed before diagnosis is deployed. Examples of pre-diagnosis activities includes classic work such as diagnostic ATPG, and DFT for increasing testability. Pre-diagnosis activities that utilize ML include test reordering and optimizing test response data collection, for example. In addition, there is work that predicts the outcome of diagnosis so that the use of compute resources can be optimized. During-diagnosis involves the algorithms (e.g., cause-and-effect, path tracing, etc.) and the underlying technologies used by the algorithms such as fault simulation. The use of ML in during-diagnosis activities generally involves learning while diagnosis executes. For example, a k-nearest neighbor model is created, evolved, and used during on-chip diagnosis to improve diagnosis outcomes. Finally, post-diagnosis includes all the activities that occur after diagnosis execution. These approaches usually involve volume diagnosis (i.e., using the outcome results of many diagnoses) to improve diagnostic resolution, that is, the number of possible failure locations (within the netlist and/or the layout). The use of ML in post-diagnosis activities is a perfect application for ML given the abundance of well-structured, labeled data from prior diagnoses, physical failure analyses, and precise fault simulations. The bulk of the work discussed lies in post-diagnosis and focusses on localization behavior identification improvement.

#### Teatro

Tutorial 2 : Silicon Lifecycle Management

MODERATOR : IOANA VATAJELU

**PRESENTER : - YERVANT ZORIAN, SYNOPSIS, US**

Abstract : To be announced

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### ETS23 - Welcome reception

19:00 – 21:00



ETS23 PROGRAM AT A GLANCE

**Monday 22**

	Auditorium	Teatro	Room 7
15:00 – 16:45	<b>TSS Tutorial 1</b> Machine Learning in Logic Circuit Diagnosis	<b>TSS Tutorial 2</b> Silicon Lifecycle Management: Trends and Solutions	
16:00 – 18:00			ETS Steering Committee meeting
16:45 – 17:15	Coffee Break (Room Grecale)		
17:15 – 19:00			
19:00 – 21:00	ETS23 Welcome Reception (Room Grecale)		

**Tuesday 23**

	Auditorium	Teatro	Room 6
9:00 – 9:30	<b>Opening Session</b>		
9:30 – 10:15	<b>KEYNOTE 1 - Silicon Lifecycle Redefines Design for Test</b> (Auditorium)		
10:15 – 11:00	Coffee Break & Poster Session 1 – PHD and Industrial Posters (Room Grecale)		
11:00 – 12:30	<b>Hyper Panel 1B</b> What do we expect from Silicon Lifecycle Management in the next 20 years? (Auditorium)	<b>Regular Session 1A</b> Tools for DNN resilience analysis (Teatro)	
12:30 – 14:00	ETS'23 Organizing Committee (Room 7)	Lunch (Room Grecale)	
14:00 – 15:30	<b>Regular Session 2A</b> Error analysis in application and unconventional computing	<b>Special Session 2C</b> Updates on functional safety standardization in autonomous systems	<b>Industrial Session 2B</b> Automatic Test Equipment
15:30 – 16:15	Coffee Break & Poster Session 2 – PHD and Industrial Posters (Room Grecale)		
16:15 – 17:45	<b>Regular Session 3A</b> AI for test	<b>Special Session 3C</b> EU projects: Emerging Technologies, Reliability and Security	<b>Industrial Session 3B</b> Automatic Test Pattern Generation
18:00 – 19:00	<b>The race for EU chip Sovereignty: where and how can test/design/EDA community help?</b> <i>followed by Wine and Cheese (Auditorium – Room Grecale)</i>		

### Wednesday 24

	Auditorium	Teatro	Room 6
8:30 - 9:15	<b>KEYNOTE 2</b> - Beyond neural networks, exploring the future of computing hardware <i>(Auditorium)</i>		
9:15 - 10:15	<b>Regular Session 4C</b> On-line testing of AI hardware	<b>Regular Session 4A</b> Resistive Memory Test and Diagnosis	<b>Industrial Session 4B</b> Analog Test
10:15 - 11:00	Coffee break & Poster Session 3 - Scientific posters <i>(Room Grecale)</i>		
11:00 - 12:30	<b>Special Session 5C</b> Introduction to RISC-V and open source hardware	<b>Hyper Panel 5B</b> Challenges for the Metaverse Hardware	<b>Regular Session 5A</b> Architecture-level security
12:30 - 14:00	Lunch <i>(Room Grecale)</i>		eTTTC meeting <i>(Room 7)</i>
14:00 - 15:30	<b>Special Session 6C</b> Introduction to RISC-V and open source hardware (II)	<b>Regular Session 6A</b> Secure building blocks	<b>Industrial Session 6B</b> Reliability Estimation
16:30	<b>Social Event</b>		

### Social Event

During Social Event, the participants will move with private boats booked by the ETS organization.

- 16:30 – departures from San Servolo island
- 16:45 – guided tour starts from Cornoldi pier
- 18:00 – Departure to Murano island from Fondamenta Nove
- 18:30 – Arrival to Murano - one hour free time
- 19:30 - Dinner offered by Infineon, main ETS23 supporter, at the Glass Cathedral in Murano**
- 23:00 – first boat back to Lido, San Marco and San Servolo
- 1:00 – second boat back to Lido, San Marco and San Servolo





### Thursday 25

	Auditorium	Teatro	Room 6
8:45 – 10:15	<b>Regular Session 7A</b> System-level test and advanced architectures	<b>PHD forum 7C</b>	<b>Industrial Session 7B</b> Miscellaneous
10:15 – 11:00	Coffee break & Poster Session 4 – Scientific posters ( <i>Grecale room</i> )		
11:00 – 12:30	<b>McCluskey Award 8C</b>	<b>Hyper Panel 8B</b> What Design for Testing strategies are envisioned for future ICs?	<b>Regular Session 8A</b> AMS-RF Design for Test & Parametric Test of Si Spin Qbit arrays
12:30 – 14:00	Lunch ( <i>Grecale Room</i> )		ETS'24 Organizing Committee ( <i>Room 7</i> )
14:00 – 15:00	Hyper Panel - Wrap Up Session (Auditorium)		
15:00 – 15:30	Closing Session (Auditorium)		

### ETS23 FRINGE WORKSHOP

#### Thursday 25

	Teatro	Room 6	Room 7
16:00 - 18:30	<b>IEEE AI-TREATS</b> 3rd IEEE Workshop on AI Hardware: Test, Reliability and Security	<b>eARTS</b> European Automotive, Reliability, Test and Safety Workshop	<b>IMTR</b> Intelligent Methods for Test and Reliability
18:30 - 20:30	Welcome Reception ( <i>Room Grecale</i> )		
20:30 – 22:30	ETS23 Organizing Committee dinner ( <i>Panoramic terrace</i> )		

#### Friday 26

	Teatro	Room 6	Room 7
8:30 - 10:00	<b>IEEE AI-TREATS</b> 3rd IEEE Workshop on AI Hardware: Test, Reliability and Security	<b>eARTS</b> European Automotive, Reliability, Test and Safety Workshop	<b>IMTR</b> Intelligent Methods for Test and Reliability
10:00 - 10:30	Coffee break & Poster Session – Workshop posters ( <i>Room Grecale</i> )		
10:30 - 12:30	<b>IEEE AI-TREATS</b>	<b>eARTS</b>	<b>IMTR</b>
12:30 - 13:30	Lunch ( <i>Room Grecale</i> )		
13:30 - 16:00	<b>IEEE AI-TREATS</b>	<b>eARTS</b>	<b>IMTR</b>

## TUESDAY, MAY 23RD, 2023

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### ETS23 Plenary Opening

CO-GENERAL CHAIR : PAOLO BERNARDI (POLITECNICO DI TORINO), DANIEL TILLE (INFINEON)

PROGRAM CHAIR : ALBERTO BOSIO (INL - ECOLE CENTRAL DE LYON)

9:00 – 9:30

Auditorium

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### Keynote 1 : Silicon Lifecycle Redefines Design for Test

9:30 – 10:15

Auditorium

PRESENTER : JANUSZ RAJSKI, SIEMENS, US

MODERATOR : ZEBO PENG (LINKOPING UNIVERSITY)

**Bio:** During his tenure at Mentor and Siemens, he has built a strong R&D organization with a focus on innovative Design for Test technologies and collaboration with leading semiconductor companies. Under his leadership, the team has developed several revolutionary, industry-first, trend-setting products: TestKompres, the first commercial test compression product, Cell-Aware Test technology which provides unprecedented test quality and accuracy of diagnosis, and Streaming Scan Network – the first commercial SoC-level structural DFT methodology. He has published more than 280 IEEE research papers and is a co-inventor of 130 US and a corresponding number of international patents. His papers and patents have over 15,000 citations and won many prestigious awards, including two Donald Pederson best paper awards for papers published in the IEEE Transactions on CAD papers. A Lifetime Fellow of the IEEE, he holds a Master of Science degree in electrical engineering from the Gdańsk University of Technology and a Ph.D. degree in electrical engineering as well as an honorary doctorate from the Poznań University of Technology. In 2003, he was awarded the prestigious title of “Professor of Science” by the President of Poland. In 2009 he received the Stephen Swerling



**Abstract :** A growing number of safety-critical and mission-critical applications require an extremely reliable operation. In automotive applications and large-scale data centers, we rely on DFT not only for manufacturing but throughout the entire silicon lifecycle. As more advanced technology nodes, especially those at 7 nm and below, and 2.5D/3D multi-die packaging is adopted, we observe new more complex parametric defects and reliability risks related to aging. Several companies reported Silent Data Corruption Errors in large-scale data centers. A closer examination of the problem shows four underlying issues: test escapes, early “infant mortality”, random/latent/aging defects, and environmental conditions that lead to malfunctions. In this talk, we review the challenges posed by these issues and examine the feasibility of emerging solutions to address them. Traditionally, we use deterministic structural tests to achieve high quality in chip manufacturing and rely on Logic BIST for in-system tests. But the test quality achieved by Logic BIST is insufficient. Can a deterministic structural test, periodically applied during in-system, achieve the required high reliability? How can the test quality be improved to reduce test escapes in manufacturing? Can stress tests be refined to reduce early mortality? Can environmental monitoring detect load conditions or aging leading to errors and prevent them from manifesting themselves?

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Poster Session 1 : PhD and Industrial Posters

10:15 – 11:00 and 15:30 - 16:15

Room Grecale – co-located with coffee break

PhD 1 : Test and Reliability of In-Memory Computing Architectures for Internet of Things

Lila AMMOURA (LIRMM - University of Montpellier)

PhD 2 : Machine Learning for Microcontroller Performance Screening

Nicolo BELLARMINO (Politecnico di Torino)

PhD 3 : Low-cost generation of test stimuli for RF devices

Kamilia TAHRAOUI (LIRMM - University of Montpellier)

PhD 4 : Taking Test Programs Connectivity to the Bit-Level

Andrea CALABRESE (Politecnico di Torino)

PhD 5 : Reporting Test Programs Connectivity In A Human-Readable Format

Lorenzo CARDONE(Politecnico di Torino)

PhD 6 : Learn Faster from Less Data: Opportunities with Hyperdimensional Computing

Paul GENSSLER(Univ. Stuttgart)

PhD 7 : Dependable Hardware for Trustworthy Artificial Intelligence

Salvatore PAPPALARDO (Politecnico di Torino)

PhD 8 : Exploring the Approximate Computing Impact on Spiking Neural Networks

Sepide SAEEDI (INL - ECL)

PhD 9 : Exploring the impact of Approximation on Reliability and performance of DNN Accelerators

Mahdi TAHERI (Tallinn University of Technology)

PhD 10 : Learning-Based Characterization Models for Quality Assurance of Emerging Memory Technologies

Xhesila XHAFA (LIRMM - University of Montpellier)

PhD 11 : Understanding and Improving GPUs' Reliability Combining Beam Experiments with Fault Simulation

Fernando FERNANDES DOS SANTOS (Rennes University IRISA/INRIA)

~~PhD 12 : Security-Aware Physical Synthesis of Integrated Circuits~~

~~Tiago DIADAMI PEREZ (Tallinn University of Technology) (withdrawn)~~

PhD 13 : Reliability and Security Assessment of Modern Embedded Devices

Annachiara RUOSPO (Politecnico di Torino)

PhD 14 : Methods to Optimize Functional Safety Assessment for Automotive Integrated Circuits

Ahmet Cagri BAGBABA (Tallinn University of Technology)

INDUSTRIAL 1 : Comparative Analysis of Object Detection Algorithms for Optical Inspection in IC Test Socket Manufacturing  
Vijayakumar THANGAMARIAPPAN, Nidhi AGRAWAL, Jason KIM, Constantinos XANTHOPOULOS (Advantest America Inc.), Ira LEVENTHAL (Advantest America, Inc.), Ken BUTLER (Advantest America Inc.), Joe XIAO (Essai Inc.)

INDUSTRIAL 2 : A Prototyping Framework for Low-cost, At-Speed Validation of I3C Controllers

Aradhana KUMARI (STMICROELECTRONICS)

INDUSTRIAL 3 : A Semi-formal approach to coverage analysis and System-on-Chip debugging

Kiran RAMPURKAR (Intel India)

INDUSTRIAL 4 : Automatic Pattern Recognition with Machine Learning For Post Silicon Measurements  
Malek BEZZINA, Daniele DARIO, Giorgia CASSETTA (Infineon)

INDUSTRIAL 5 : Functional Safety methodology for ISO26262 certification  
Victor ARRIBAS (Rambus)

INDUSTRIAL 6 : Intensive Verification Framework based on Virtual Platform for Incremental Regression Test  
Jeehoon CHOI (Samsung Electronics)

INDUSTRIAL 7 : Mitigation of Parasitic Dynamic Power Dissipation of Scan Buffers in Functional Mode  
Ankur BAL (STMICROELECTRONICS)

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Session 1B : Hyper Panel 1 - What do we expect from Silicon Lifecycle Management in the next 20 years?

11:00 – 12:30

Auditorium

MODERATOR : MEHDI TAHOORI (KIT)

PANELISTS :

RALF ARNOLD

LEAD PRINCIPAL - TEST CONCEPT ENGINEERING AT MICROCONTROLLER DEPARTMENT AT INFINEON TECHNOLOGIES

JANUSZ RAJSKI

VICE PRESIDENT OF ENGINEERING, TESSENT, SIEMENS

HANS-JOACHIM WUNDERLICH

FULL PROFESSOR AT UNIVERSITY OF STUTTGART

YERVANT ZORIAN

CHIEF ARCHITECT AND FELLOW AT SYNOPSIS

Session 1A : Tools for DNN resilience analysis

11:00 – 12:30

Teatro

MODERATOR : MARIA MICHAEL (UNIVERSITY OF CYPRUS), HARALAMPOS STRATIGOPOULOS (SORBONNE UNJVERSIÈ – LIP6)

SCI-FI: a Smart, aCcurate and unIntrusive Fault-Injector for Deep Neural Networks

Gabriele GAVARINI, Annachiara RUOSPO, ERNESTO SANCHEZ (Politecnico di Torino)

DeepVigor: Vulnerability Value RanGes and FactORs for DNNs' Reliability Assessment

Mohammad Hasan AHMADILIVANI, Mahdi TAHERI, Jaan RAIK (Tallinn University of Technology), Masoud DANESHTALAB (Mälardalen University), Maksim JENIHHIN (Tallinn University of Technology)

harDNNing: a machine-learning-based framework for fault tolerance assessment and protection of DNNs

Marcello TRAIOLA (National Institute for Research in Digital Science and Technology), Angeliki KRITIKAKOU (Univ Rennes, INRIA, Irisa), Olivier SENTIEYS (INRIA)

Lunch

12:30 – 14:00

Room Grecale – co-located with supporters' area

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Session 2A : Error analysis in application and unconventional computing paradigm

14:00 – 15:30

**Auditorium**

MODERATOR : ANGELIKI KRITIKAKOU (UNIVERSITY OF RENNES), HANS-JOACHIM WUNDERLICH (UNIVERSITÄT STUTTGART)

Error Resilient Transformers: A Novel Soft Error Vulnerability Guided Approach to Error Checking and Suppression  
Kwondo MA, Chandramouli AMARNATH, Abhijit CHATTERJEE (Georgia Institute of Technology)

Understanding Permanent Hardware Failure Effects in Deep Learning Training Systems  
Yi HE (U of Chicago), Yanjing LI (University of Chicago)

DEV-PIM: Dynamic Execution Validation with Processing-in-Memory  
Alperen BOLAT (Queen University Belfast), Yahya Can TUĞRUL, Seyyid Hikmet ÇELİK (TOBB University of Economics And Technology), Sakir SEZER (Queen University Belfast), Marco OTTAVI (Twente U.), Ergin OĞUZ (TOBB University of Economics And Technology)

Session 2C : Updates on functional safety standardization in autonomous systems

14:00 – 15:30

**Teatro**

ORGANIZER: SELMA SAIDI (TECHNICAL UNIVERSITY OF HAMBURG)  
MODERATOR: TO BE ANNOUNCED

Session 2B : Industrial 1 - ATE  
14:00 – 15:30

**Room 6**

MODERATOR : TO BE ANNOUNCED

Alternative Digital ATE  
Ric DOKKEN (Roguevation, Inc.)

Expediting Test Program Development with Teradynes PortBridge Tools and Superior User Experience  
Richard FANNING, Mun-Jun LEOW (Teradyne)

Automotive MCU Temperature Sensor Trimming via PTAT  
Ralf ARNOLD (Infineon Technologies)

Vendor Presentation :  
*INFINEON*

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Poster Session 2 : PhD and Industrial Posters

15:30 - 16:15

Room Grecale – co-located with coffee break

See Poster Session 1 - [Poster Session 1 : PhD and Industrial Posters](#)

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**Session 3A : AI for test**

16:15 - 17:45

**Auditorium**

MODERATOR : JENNIFER DWORAK  
(SMU, LYLE SCHOOL OF ENGINEERING),  
LIVIU MICLEA (CLUJ NAPOCA  
UNIVERSITY)

**Semi-Supervised Deep Learning  
for Microcontroller**

Performance Screening

Nicolo' BELLARMINO, Riccardo  
CANTORO (Politecnico di Torino),  
Martin HUCH (Infineon  
Technologies AG), Tobias KILIAN  
(Infineon Technologies AG,  
Technical University of Munich),  
Ulf SCHLICHTMANN (TUM),  
Giovanni SQUILLERO (Politecnico  
di Torino)

\*Best paper candidate

**Test-Point Insertion for Power-  
Safe Testing of Monolithic 3D  
ICs using Reinforcement  
Learning**

Shao-Chun HUNG (Duke  
University), Arjun CHAUDHURI  
(Duke University), Krishnendu  
CHAKRABARTY (Arizona State  
University)

\*Best paper candidate

**Learning Electrical Behavior of  
Core Interconnects for System-  
Level Crosstalk Prediction**

Katayoon BASHARKHAH, Raheleh  
sadaat MIRHASHEMI, Nooshin  
NOSRATI, Mohammad javad ZARE  
(University of Tehran),  
Zainalabedin NAVABI (Worcester  
Polytechnic Institute)

**Session 3C : EU Projects:  
Emerging Technologies,  
Reliability and Security**

16:15 - 17:45

**Teatro**

MODERATOR : MAKSIM JENIHHIN  
(TALTECH)

**CONVOLVE: Seamless design of  
Smart, reliable and secure Edge  
Processors**

Said Hamdioui (TU Delft)

NEUROPULS: NEUromorphic  
energy-efficient secure  
accelerators based on Phase  
change materials augmented  
silicon photonicS  
Fabio Pavanello (INL/CNRS)

VITAMIN-V: Virtual Environment  
and Tool-Boxing for  
Trustworthy Development of  
RISC-V Based Cloud Services  
Stefano Di Carlo (Politecnico di  
Torino)

**Session 3B : Industrial 2 -  
ATPG**

16:15 - 17:45

**Room 6**

MODERATOR : LEE HARRISON (SIEMENS)

Conflict-driven Structural  
Learning Towards Higher  
Coverage Rate in ATPG  
**Huiling ZHEN (Huawei)**

Efficient Test and Diagnosis  
Pattern Generation for Large  
Numbers of Inter-Die  
Interconnects in Chiplet-Based  
Packages

**Po-Yao CHUANG (IMEC)**

Novel Deterministic  
Manufacturing Scan Testing  
Architecture Based on High-  
Speed SerDes IO  
**Haitao FU (Huawei Technologies  
Co., Ltd)**

Vendor Presentation :  
*Implementing design for test  
(DFT) in 2.5/3D designs using  
Tessent Multi-die*  
**Haitao FU (Huawei Technologies  
Co., Ltd)**



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Plenary Panel : The race for EU chip Sovereignty: where and how can test/design/EDA community help?

18:00 – 19:30

Auditorium

MODERATOR : SAID HAMDIOUI (TU DELFT)

**PANELISTS : TO BE ANNOUNCED**

Abstract : To be announced

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Aperitif offered by ETS23

19:30 – 20:00

Grecale

## WEDNESDAY, MAY 24TH, 2023

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Keynote 2 : Beyond neural networks, exploring the future of computing hardware

8:30 – 9:15

Auditorium

PRESENTER : Valeria Bertacco, University of Michigan, US

MODERATOR : MATTEO SONZA REORDA (POLITECNICO DI TORINO)

**Bio** : Valeria Bertacco is the Mary Lou Dorf Professor of Computer Science and Engineering, and a Thurnau Professor at the University of Michigan. She is also Adjunct Professor of Computer Engineering at the Addis Ababa Institute of Technology. Her research interests are in the area of computer design, with emphasis on specialized architecture solutions and design viability, in particular reliability, validation, and hardware-security assurance. Her research endeavors are supported by the Applications Driving Architectures (ADA) Research Center, which Valeria directs. The ADA Center, sponsored by a consortium of semiconductor companies, has the goal of reigniting computing systems design and innovation for the 2030-2040s decades, through specialized heterogeneity, domain-specific language abstractions, and new silicon devices that show benefit to applications.



Valeria joined the University of Michigan in 2003. She currently serves as the Vice Provost for Engaged Learning at the University of Michigan, supporting all co-curricular engagements and international partnerships for the institution, and facilitating the work of several central units, whose goals range from promoting environmental sustainability, to the promotion of the arts in research universities, and to increasing the participation of gender minorities in the academy.

**Abstract** : The success of specialized hardware in enabling ML acceleration has been nothing short of remarkable. Today, neural network accelerators have matured into industry-strength products. But there is more to computing than meets the neural network. To address the future needs of computing, a few pressing challenges must be urgently addressed, and the hardware community is critical in clearing the path to that future. In this talk, I will focus on three key challenges that computing is facing today: data processing scalability, privacy, and environmental sustainability. Along with those, I will outline new opportunities that the related solutions offer to the testing community.

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Session 4C : On-line testing of AI hardware

9:15 – 10:15

**Auditorium**

MODERATOR : SYBILLE HELLEBRAND (PADERBORN UNIVERSITY), GIULIO GARBANDELLA (SYNOPSISYS)

On-Line Testing of Neuromorphic Hardware Theofilos SPYROU (Sorbonne Université, CNRS, LIP6), Haralampos STRATIGOPOULOS (Sorbonne Univ., CNRS, LIP6)

**\*Best paper candidate**

Image Test Libraries for the on-line self-test of functional units in GPUs running CNNs

Annachiara RUOSPO, Gabriele GAVARINI, Antonio PORCIA, Matteo SONZA REORDA, ERNESTO SANCHEZ (Politecnico di Torino), Riccardo MARIANI, Aribido JOSEPH (Nvidia Corporation), Jyotika ATHAVALE (NVIDIA)

**\*Best paper candidate**

Session 4A : Resistive Memory Test and Diagnosis

9:15 – 10:15

**Teatro**

MODERATOR : LETICIA MARIA BOLZANI PÖHLS (RWTH AACHEN UNIVERSITY), ARNAUD VIRAZEL (LIRMM)

Data Background-Based Test Development for All Interconnect and Contact Defects in RRAMs Hanzhi XUN, Moritz FIEBACK (Delft), Sicong YUAN, Ziwei ZHANG (Technische Universiteit Delft), Mottaqiallah TAOUIL, Said HAMDIOUI (Delft University of Technology)

Online Fault Detection and Diagnosis in RRAM Moritz FIEBACK, Filip BRADARI, Mottaqiallah TAOUIL, Said HAMDIOUI (Delft University of Technology)

Session 4B : Industrial 3 - Analog Test

9:15 – 10:15

**Room 6**

MODERATOR : CLAUDIA BERTANI (STM)

Reusing tests during IC development and delivery Stephen SUNTER (Siemens Digital Industries Software)

Ultra-low jitter reduction methods for high speed test instrumentation David KEEZER (Georgia Institute of Technology)

Utilizing System Level Test to Achieve High-throughput, Automated RF Testing John TOSCANO, Peter REICHERT (Teradyne)

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Poster Session 3 : Scientific posters

10:15 - 11:00

Room Grecale – co-located with coffee break

POSTER 1 : A Resilience Framework for Synapse Weight Errors and Firing Threshold Perturbations in RRAM Spiking Neural Networks

Anurup SAHA (Georgia Tech), Chandramouli AMARNATH, Abhijit CHATTERJEE (Georgia Institute of Technology)

POSTER 2 : A Side-Channel Attack on a Hardware Implementation of CRYSTALS-Kyber Yanning JI (KTH Royal Institute of Technology), Ruize WANG (Royal Institute of Technology), Kalle NGO (KTH Royal Institute of Technology), Elena DUBROVA, Linus BACKLUND (Royal Institute of Technology)

POSTER 3 : An unprotected RISC-V Soft-core processor on an SRAM FPGA: Is it as bad as it sounds?

Bruno ENDRES FORLIN, Wouter VAN HUFFELEN (University of Twente), Cazzaniga CARLO (Rutherford Appleton Laboratory-ISIS), Paolo RECH (University of Trento), Nikolaos ALACHIOTIS (University of Twente), Marco OTTAVI (Twente U.)

POSTER 4 : Attacking Memristor-mapped Graph Neural Network by Inducing Slow-to-Write Errors

Ching-Yuan CHEN (Duke University), Biresh Kumar JOARDAR (University of Houston), Janardhan Rao DOPPA, Partha Pratim PANDE (Washington State University), Krishnendu CHAKRABARTY (Arizona State University)

POSTER 5 : Automating Greybox System-Level Test Generation

Denis SCHWACHHOFER, Maik BETKA, Steffen BECKER, Wagner STEFAN (University of Stuttgart), Matthias SAUER (Advantest), Ilia POLIAN (University of Stuttgart)

POSTER 6 : Automating the Generation of Functional Stress Inducing Stimuli for Burn-In Testing

Nikolaos DELIGIANNIS (Politecnico di Torino), Tobias FALLER (University of Freiburg), Zhou CHENGHAN, Riccardo CANTORO, Matteo SONZA REORDA (Politecnico di Torino), Bernd BECKER (University of Freiburg)

POSTER 7 : BiSTAHL: A Built-In Self-Testable Soft-Error-Hardened Scan-Cell

Stefan HOLST (Kyushu Institute of Technology), Ruijun MA (Anhui University of Science and Technology), Xiaoqing WEN (Kyushu Institute of Technology), Aibin YAN (Anhui University), Hui XU (Anhui University of Science and Technology)

POSTER 8 : BitFREE: On Significant Speedup and Security Applications of FPGA Bitstream Format Reverse Engineering

Tao ZHANG, Mark TEHRANIPOOR, Farimah FARAHMANDI (University of Florida)

POSTER 9 : Counterfeit Detection by Semiconductor Process Technology Inspection

Matthias LUDWIG, Ann-Christin BETTE, Bernhard LIPPMANN (Infineon Technologies AG), Georg SIGL (Technical University of Munich)

POSTER 10 : Criticality Analysis of Ring Oscillators in FPGA Bitstreams

Jayeeta CHAUDHURI (Duke University), Krishnendu CHAKRABARTY (Arizona State University)

POSTER 11 : Density-oriented diagnostic data compression strategy for characterization of embedded memories in Automotive Systems-on-Chip

Giorgio INSINGA, Matteo BATTILANA (Politecnico di Torino), Matteo COPPETTA, Nellina MAUTONE, Giambattista CARNEVALE, Rudolf ULLMANN, Massimo GILTRELLI, Pierre SCARAMUZZA (Infineon)

POSTER 12 : FINaL: Driving High-Level Fault Injection Campaigns with Natural Language

Khaled Galal Abdelwahab ABDELAZIZ (TU Hamburg), Ralph GÖRGEN (NXP Semiconductors), GOERSCHWIN FEY (TU Hamburg)

POSTER 13 : Global Tuning for System Performance Optimization of RF MIMO Radars

Ferhat Can ATAMAN, Muslum Emir AVCI (Arizona State University), Chethan KUMAR Y.B. (Texas Instruments), Sule OZEV (Arizona State University)

POSTER 14 : Harvesting Wasted Clock Cycles for Efficient Online Testing

Eslam YASSIEN, Yongjia XU, Hui JIANG (Southern Methodist University), Thach NGUYEN (University of St. Thomas), Jennifer DWORAK, Theodore MANIKAS (Southern Methodist University), Kundan NEPAL (University of St. Thomas)

POSTER 15 : High-coverage analog IP block test generation methodology using low-cost signal generation and output response analysis

Jhon GOMEZ (KU LEUVEN), Nektar XAMA (KULeuven), Anthony COYETTE (ON Semiconductor), Ronny VANHOOREN, Wim DOBBELAERE (onsemi), Georges GIELEN (KU Leuven)

Session 5C : Introduction to RISC-V and open source hardware

11:00 – 12:30

Auditorium

MODERATOR : MARCELLO TRAIOLA (IRISA, RENNES)

The first 10 years of PULP Platform and open source hardware approach

Frank K. Gürkaynak (ETH Zürich)

Redundancy schemes for PULP systems

Yvan Tortorella (University of Bologna)

Practical implementations and cooperations for reliable architectures using open source hardware

Michael Rogenmoser (ETH Zürich)

Building a Resilient and Dependable RISC-V System

Markus Ulbricht (IHP Microelectronics)

Session 5B : Hyper Panel 2 - Challenges for the Metaverse Hardware

11:00 – 12:30

Teatro

CO-ORGANIZERS : CECILIA METRA, JEEWIK RANAWEERA, STEVE DUKES

MODERATOR : CECILIA METRA (UNIVERSITÀ DI BOLOGNA)

PANELISTS:

ALESSANDRO CREMONESI  
VP AT STMICROELECTRONICS

RICCARDO LOCATELLI  
FUNCTIONAL SAFETY ARCHITECT AT INTEL CORPORATION

JEEWIK RANAWEERA  
EX-PRINCIPAL HARDWARE ENGINEER AT ORACLE

ANNA ZAKRZEWSKA  
SENIOR PRINCIPAL ENGINEER AT DELL TECHNOLOGIES

YERVANT ZORIAN  
CHIEF ARCHITECT AND FELLOW AT SYNOPSIS

Session 5A : Architecture-level security

11:00 – 12:30

Room 6

MODERATOR : CÉDRIC MARCHAND (ECOLE CENTRALE LYON - INL), JOHANNA SEPULVEDA (AIRBUS)

Power Side-Channel Attacks and Countermeasures on Computation-in-Memory Architectures and Technologies

Brojogopal SAPUI, Jonas KRAUTTER (Karlsruhe Institute of Technology, Germany), Mahta MAYAHINIA, Atousa JAFARI (KIT university), Dennis GNAD (Karlsruhe Institute of Technology), Sergej MESCHKOV (Karlsruhe Institute of Technology (KIT)), Mehdi TAHOORI (Karlsruhe Institute of Technology)  
**\*Best Paper Candidate**

Secrets Leaking Through Quicksand: Covert Channels in Approximate Computing

Lorenzo MASCIULLO, Roberto PASSERONE (University of Trento), Francesco REGAZONI (ALaRI), Ilia POLIAN (University of Stuttgart)

Increasing SAT-Resilience of Logic Locking Mechanisms using Formal Methods

Marcel MERTEN, Sebastian HUHN, Rolf DRECHSLER (University of Bremen)

Lunch

12:30 – 14:00

Room Grecale – co-located with supporters' area

Session 6C : Introduction  
to RISC-V and open  
source hardware

14:00 – 15:30

**Auditorium**

MODERATOR : ALESSANDRO  
SAVINO (POLITECNICO DI TORINO)

System-level Fuzzed Testing  
for RISC-V

Ilia Polian (U. Stuttgart)

SELENE: A RISC-V Platform  
for safety-related  
Applications

Carles Hernandez (UP.  
Valencia)

RISC-V for Security  
Applications

Nele Mentens (U. Leiden)

Session 6A : Secure  
building blocks

14:00 – 15:30

**Teatro**

MODERATOR : MARIE LISE FLOTTES  
(LIRMM), FRANCESCO REGAZZONI  
(UVA AMSTERDAM AND ALARI  
LUGANO)

High Throughput and  
Energy Efficient SHA-2 ASIC  
Design for Continuous  
Integrity Checking  
Applications

Asimina KOUTRA, Vasileios  
TENENTES (University of  
Ioannina)

SiCBit-PUF: Strong in-Cache  
Bitflip PUF Computation for  
Trusted SoCs

Athanasios XYNOS, Vasileios  
TENENTES, Yiorgos  
TSIATOUHAS (University of  
Ioannina)

Online Reliability Evaluation  
Design: Select Reliable CRPs  
for Arbiter PUF and Its  
Variants

Chaofang MA, Jianan MU  
(State Key Laboratory of  
Processors, Institute of  
Computing Technology,  
Chinese Academy of Sciences;  
CASTEST), Jing YE (Institute of  
Computing Technology,  
Chinese Academy of  
Sciences), Shuai CHEN (Rock-  
Solid Security Lab), Yuan CAO  
(Hohai University), HUAWEI LI  
(Chinese Academy of  
Sciences), Xiaowei LI (Institute  
of Computing Technology,  
CAS)

Session 6B : Industrial 4 -  
Reliability Estimation

14:00 – 15:30

**Room 6**

MODERATOR : GIUSEPPE RUMI  
(STMICROELECTRONICS)

Fault injection strategies:  
identifying HW failures with  
functional impact

Iban GUINEBERT (ONERA)

Predictive Maintenance in  
the Context of Automotive  
Functional Safety

Andrea MATTEUCCI  
(proteanTecs)

Vendor Presentation :

Breaking down the barriers  
of In-System Test with  
Silicon Lifecycle Monitoring  
Yervant ZORIAN (Synopsys)

**Social Event**

16:00 – 23:00

Including dinner at Murano Island – Students are admitted



## THURSDAY, MAY 25TH, 2023

### Session 7A : System-level test and advanced architectures

8:45 – 10:15

#### Auditorium

MODERATOR : RICCARDO CANTORO (POLITO), BERND BECKER (UNIV. FREIBURG)

#### Evaluating the Prevalence of SFUs in the Reliability of GPUs

Josie RODRIGUEZ CONDIA, Juan GUERRERO (Politecnico di Torino), Edwar J. PATINO N. (Universidad Pedagogica y Tecnologica de Colombia), Robert LIMAS SIERRA, Matteo SONZA REORDA (Politecnico di Torino)

#### Hybrid Ring Generators for In-System Test Applications

Jerzy TYSZER (Poznan University of Technology), Janusz RAJSKI, Maciej TRAWKA (Siemens Digital Industries Software), Bartosz WLODARCZAK (Poznan University of Technology)

#### Constraint-Based Automatic SBST Generation for RISC-V Processor Families

Tobias FALLER (University of Freiburg), Nikolaos DELIGIANNIS (Politecnico di Torino), Markus SCHWOERER (University of Freiburg), Matteo SONZA REORDA (Politecnico di Torino), Bernd BECKER (University of Freiburg)

### Session 7C : PhD Forum

8:45 – 10:15

#### Room 6

MODERATOR : ANGELIKI KRITIKAKOU (UNIVERSITY OF RENNES), PAOLO RECH (TRENTO UNIVERSITY)

Thesis 1 : Test and Reliability of In-Memory Computing Architectures for Internet of Things  
Lila AMMOURA (LIRMM - University of Montpellier)

Thesis 2 : Machine Learning for Microcontroller Performance Screening  
Nicolo BELLARMINO (Politecnico di Torino)

Thesis 3 : Low-cost generation of test stimuli for RF devices  
Kamilia TAHRAOUI (LIRMM - University of Montpellier)

Thesis 4 : Taking Test Programs Connectivity to the Bit-Level  
Andrea CALABRESE (Politecnico di Torino)

Thesis 5 : Reporting Test Programs Connectivity In A Human-Readable Format  
Lorenzo CARDONE (Politecnico di Torino)

Thesis 6 : Learn Faster from Less Data: Opportunities with Hyperdimensional Computing  
Paul GENSSLER (Univ. Stuttgart)

### Session 7B : Industrial 4 – Miscellaneous

8:45 – 10:15

#### Room 7

MODERATOR : CARLO PROTTI MELANO (ALLEGRO MICROSYSTEMS)

#### TAL: Test Automation Language

Tiago MOITA (SILICONGATE LDA), Marcelino SANTOS, André AGOSTINHO (IST-ULisboa / INESC-ID / SILICONGATE)

#### Probe Card Interface: A safety system for HI/HV testing of power semiconductor devices

Marco Marcinnò, Carlo CIANFEROTTI, Alberto RAVA (CREA SRL), Ruo Roch MASSIMO (Politecnico di Torino)

#### Multi-Site Air Distribution Chamber Design for ATE

W ALBAN IMMANUEL (Infineon Technologies), Hariharan GNANASEKARAN (Cypress Semiconductor), JEY NITHYANANDAM (Infineon Technologies)

#### Enabling fast post-Si test case development using Virtual Prototyping for a mixed-signal gate driver IC

Manuel HARRANT, Thomas NIRMAIER, Olivier BARONDEAU, Wendy YOU, Martin SOELKNER (Infineon), Georg PELZ (Infineon Technologies, Neubiberg, Germany)



Thesis 7 : Dependable  
Hardware for Trustworthy  
Artificial Intelligence  
**Salvatore PAPPALARDO**  
(Politecnico di Torino)

Thesis 8 : Exploring the  
Approximate Computing  
Impact on Spiking Neural  
Networks  
**Sepide SAEEDI (INL - ECL)**

Thesis 9 : Exploring the  
impact of Approximation on  
Reliability and performance  
of DNN Accelerators  
**Mahdi TAHERI (Tallinn  
University of Technology)**

Thesis 10 : Learning-Based  
Characterization Models for  
Quality Assurance of  
Emerging Memory  
Technologies  
**Xhesila XHAFA (LIRMM -  
University of Montpellier)**

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**Poster Session 4 : Scientific posters**

10:15 - 11:00

Room Grecale – co-located with coffee break

POSTER 16 : Interconnect Approximate Computing: Balancing Performance, Power, and Safety

Abdalrhman BADRAN, Somayeh SADEGHI-KOHAN, Jan Dennis REIMER, Sybille HELLEBRAND (University of Paderborn)

POSTER 17 : Intra-cell Resistive-Open Defect Analysis on a Foundry 8T SRAM-based IMC Architecture

Lila AMMOURA, Marie-Lise FLOTTES, Patrick GIRARD (LIRMM), Jean-Philippe NOEL (CEA), Arnaud VIRAZEL (LIRMM)

POSTER 18 : Learn to Tune: Robust Performance Tuning in Post-Silicon Validation  
Peter DOMANSKI (IPVS (University Stuttgart)), Raphaël LATTY (Advantest (Böblingen)), Pflueger DIRK (University of Stuttgart)

POSTER 19 : Micro-Architectural features as soft-error induced fault executions markers in embedded safety-critical systems: a preliminary study

Deniz KASAP (Bilkent University), Alessio CARPEGNA, Alessandro SAVINO, Stefano DI CARLO (Politecnico di Torino)

POSTER 20 : On Using Cell-Aware Methodology for SRAM Bit Cell Testing  
Xhesila XHAFA (LIRMM), Aymen LADHAR, Eric FAEHN (STM), Lorena ANGHEL (Grenoble-INP), Gregory DI PENDINA (CNRS, CEA, INAC-SPINTEC), Patrick GIRARD, Arnaud VIRAZEL (LIRMM)

POSTER 21 : On-chip Electromigration Sensor for Silicon Lifecycle Management of Nanoscale VLSI

Mahta MAYAHINIA (KIT university), Mehdi TAHOORI (Karlsruhe Institute of Technology), Grigor TSHAGHARYAN, Gurgen HARUTYUNYAN, Yervant ZORIAN (Synopsys)

POSTER 22 : Online Fault-Tolerance for Memristive Neuromorphic Fabric Based on Local Approximation

Soyed Tuhin AHMED, Roman RAKHMATULLIN, Mehdi TAHOORI (Karlsruhe Institute of Technology)

POSTER 23 : Online Performance Monitoring of Neuromorphic Computing Systems

Abhishek Kumar MISHRA, Nagarajan KANDASAMY, Anup Kumar DAS (Drexel University)

POSTER 24 : Physical-aware interconnect testing and repairing of Chiplets

Changming CUI (Hisilicon), xu TUANHUI (hisilicon), Fu HAITAO, Junlin HUANG (Hisilicon)

POSTER 25 : PSC-Watermark: Power Side Channel Based IP Watermarking Using Clock Gates

Upoma DAS, Mohammad RAHMAN, N. Nalla ANANDAKUMAR, Kimia ZAMIRI AZAR, Fahim RAHMAN, Mark TEHRANIPOOR, Farimah FARAHMANDI (University of Florida)

POSTER 26 : SET Effects on Quasi Delay Insensitive and Synchronous Circuits  
Zaheer TABASSAM (TU Wien), Andreas STEININGER (TU Vienna)

POSTER 27 : Spotlight: An Impairing Packet Transmission Attack Targeting Specific Node in NoC-based TCMP

Jiaoyan YAO (Nanjing University of Aeronautics and Astronautics), Ying ZHANG, Yifeng HUA, Yuanxiang LI, Jizhong YANG (College of Electronic and Information Engineering, Nanjing University of Aeronautics and Astronautics), xin CHEN (Nanjing University of Aeronautics and Astronautics)

POSTER 28 : Stimuli Generation for IC Design Verification using Reinforcement Learning with an Actor-Critic Model

Stijn TWEETHUYSEN, Guido ADRIAANS (Prodrive Technologies), Manil Dev GOMONY (Electronic Systems Group)

POSTER 29 : Synthesis of IJTAG Networks for  
Multi-Power Domain Systems on Chips  
Payam HABIBY (DFKI), Natalia LYLINA (Institute of  
Computer Architecture and Computer  
Engineering), Chih-Hao WANG (National Sun Yat-  
sen University), Hans-Joachim WUNDERLICH  
(Universitat Stuttgart), Sebastian HUHN, Rolf  
DRECHSLER (University of Bremen)

Session 8C : McCluskey Award

11:00 – 12:30

Auditorium

MODERATOR : ARNAUD VIRAZEL (LIRMM), ANNE MEIXNER (ENG.DAUGHTERS)

PhD 11 : Understanding and Improving GPUs' Reliability  
Combining Beam Experiments with Fault Simulation  
Fernando FERNANDES DOS SANTOS (Rennes University IRISA/INRIA)

~~PhD 12 : Security Aware Physical Synthesis of Integrated Circuits~~

~~Tiago DIADAMI PEREZ (Tallinn University of Technology) (withdrawn)~~

PhD 13 : Reliability and Security Assessment of Modern Embedded Devices  
Annachiara RUOSPO (Politecnico di Torino)

PhD 14 : Methods to Optimize Functional Safety Assessment for Automotive Integrated Circuits  
Ahmet Cagri BAGBABA (Tallinn University of Technology)

Session 8B : Hyper Panel 3 - What Design for Testing strategies are envisioned for future ICs?

11:00 – 12:30

Room 7

MODERATOR : TERESA MCLAURIN (ARM)

PANELISTS:

MATTEO COPPETTA  
*LEAD PRINCIPAL SOFTWARE BASED FUNCTIONAL TEST AT INFINEON TECHNOLOGIES*

ANTHONY COYETTE  
*MANAGER OF TEST METHODOLOGY ENGINEERING AT ONSEMI*

JENNIFER DWORAK  
*FULL PROFESSOR AT SMU, LYLE SCHOOL OF ENGINEERING*

STEPHAN EGGERSGLUESS  
*SENIOR SOFTWARE ARCHITECT AT SIEMENS EDA*

MATTHIAS SAUER  
*APPLIED RESEARCH PROJECT MANAGER AT ADVANTEST*

Session 8A : AMS-RF Design for Test & Parametric Test of Si Spin Qbit arrays

11:00 – 12:30

Room 6

MODERATOR : FLORENCE AZAÏS (LIRMM), STEPHEN SUNTER (MENTOR GRAPHICS)

Mismatch Measurement for MIMO mm-Wave Radars via Simple Power Monitors  
Ferhat Can ATAMAN, Mohammad ALADSANI, George TRICHOPOLOUS (Arizona State University), Chethan KUMAR Y.B. (Texas Instruments), Sule OZEV (Arizona State University)  
**\*Best Paper Candidate**

A Single-Event Latchup setup for high-precision AMS circuits  
Gildas LEGER (IMSE-CNM), Eduardo PERALIAS (Instituto de Microelectronica de Sevilla (IMSE-CNM)), Antonio GINES (IMSE-CNM (CSIC, Universidad de Sevilla)), Valentin GUTIERREZ, Carlos DOMINGUEZ (IMSE-CNM), Maria Angeles JALON, Luis CARRANZA (Alter)

Study of Transistor Metrics for Room-Temperature Screening of Single Electron Transistors for Silicon Spin Qubit Applications  
Francesco LORENZELLI, Asser ELSAYED, Clement GODFRIN, Alexander GRILL, Stefan KUBICEK, Ruoyu LI, Michele STUCCHI, Danny WAN, Kristiaan DE GREVE, Erik Jan MARINISSEN (IMEC), Georges GIELEN (KU Leuven)

Lunch

12:30 – 14:00

Room Grecale – co-located with supporters' area

Hyper Panel : Wrap-Up

14:00 – 15:30

Auditorium

MODERATOR : DAVIDE APPELLO (STMICROELECTRONICS)

PANELISTS :

MEHDI TAHOORI

FULL PROFESSOR AND CHAIR OF DEPENDABLE NANO COMPUTING AT KARLSRUHE INSTITUTE OF TECHNOLOGY

CECILIA METRA

IEEE DIRECTOR/DIVISION V DELEGATE, 2022-2023 - IEEE COMPUTER SOCIETY PRESIDENT 2019 - PROFESSOR - DEPUTY PRESIDENT ENGINEERING SCHOOL, UNIVERSITY OF BOLOGNA

TERESA MCLAURIN

FELLOW AND SENIOR DIRECTOR OF DFT ARCHITECTURE AT ARM

ETS23 Closing Session

15:00 – 16:00

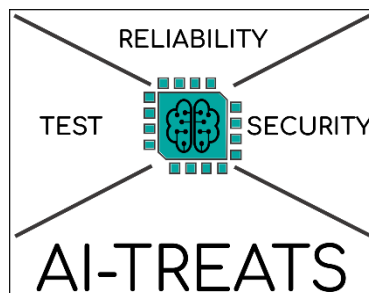
Auditorium

Workshops

16:00 – 18:30

**IEEE WORKSHOP ON AI  
HARDWARE: TEST,  
RELIABILITY AND SECURITY  
(AI-TREATS)**

TEATRO



Here you can visit the official website of the workshop:

<https://ai-treats-workshop.aalto.fi/>

**EUROPEAN AUTOMOTIVE  
RELIABILITY, TEST & SAFETY  
WORKSHOP (EARTS)**

ROOM 6

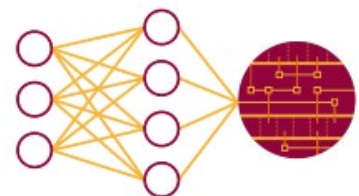


Here you can visit the official website of the workshop:

<https://cas.polito.it/eARTS2023/>

**WORKSHOP ON  
INTELLIGENT METHODS FOR  
TEST AND RELIABILITY  
(IMTR'23)**

ROOM 7



Here you can visit the official website of the workshop:

<https://www.gs-imtr.uni-stuttgart.de/imtr23/>



FRIDAY, MAY 26TH, 2023

**Workshops Day 2**

Workshops Schedule

**Thursday, 4:00-6:30 PM**

Welcome Reception at 18:30 PM

**Friday, 8:30-4:00 PM**

Coffee Break (10 - 10:30 AM)

Lunch Break (12:30 - 13:30 PM)

Workshops Welcome Reception

*18:30 – 20:30*

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## IEEE WORKSHOP ON AI HARDWARE: TEST, RELIABILITY AND SECURITY (AI-TREATS)

ORGANIZERS : HARALAMPOS-G. STRATIGOPOULOS (SORBONNE UNIVERSITY, CNRS, LIP6, FRANCE), IOANA VATAJELU (GRENOBLE ALPES UNIVERSITY, CNRS, GRENOBLE INP, TIMA, FRANCE), FEI SU (INTEL, USA), MARTIN ANDRAUD (AALTO UNIVERSITY, FINLAND)

Teatro

Here you can visit the official website of the workshop: <https://ai-treats-workshop.aalto.fi/>

Recent advances in Artificial Intelligence (AI), in particular deep learning, have led to numerous applications, including computer vision, speech recognition, natural language processing, robotics, etc. Autonomous vehicles are also afoot and AI will be the core enabling technology. In parallel, there is intense activity in designing dedicated hardware for AI. On one hand, AI hardware accelerators are demanded to support the tremendous processing power, unprecedented speed, and memory costs that deep neural networks require so as to realize their full potential. On the other hand, there is a large incentive for moving the AI algorithms execution from the cloud into the edge devices, i.e. Internet-of-Things (IoT) devices, in particular for meeting data confidentiality and network bandwidth requirements and eliminating the communication latency. Edge devices are expected to include local 3ETS FRINGE WORKSHOP PR | v.0.9AI processing, yet this is challenging as an edge device is a resource-constrained environment. AI hardware design efforts rapidly evolve exploring various architectures (e.g., machine learning-based, spiking), design flavors (e.g., digital, mixed analog-digital), and emerging technologies (e.g., memristive devices arranged into crossbars to implement efficiently the multiply-add matrix operations in neural networks). The aim of this Workshop is to focus particularly on the following emerging problems pertaining to AI hardware: Testing: fault modelling, fault simulation, test generation, post-manufacturing testing, design-for-test, built-in self-test, on-line testing, fault diagnosis. Reliability: reliability analysis, design-for-reliability, fault-tolerance, self-repair, functional safety. Hardware security and trust: IP/IC piracy, hardware Trojans, side-channel attacks, fault injection attacks.

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## IEEE EUROPEAN AUTOMOTIVE RELIABILITY, TEST & SAFETY WORKSHOP (EARTS)

GENERAL CHAIRS : YERVANT ZORIAN (SYNOPTIS, US) AND DAVIDE APPELLO (STMICROELECTRONICS, IT)

PROGRAM CHAIR : RICCARDO CANTORO (POLITECNICO DI TORINO, IT) AND WIM DOBBELEARE (ONSEMI, BE)

Room 7

Here you can visit the official website of the workshop: <https://cas.polito.it/eARTS2023/>

Automotive electronics is becoming more and more relevant in the daily life, especially with the advent of the autonomous driving. People will become 100% dependent on the proper operation of the electronic systems. The 3rd European Automotive Reliability, Test and Safety workshop (eARTS) intends to focus on test, reliability, and safety of automotive electronics, including IC design, test development, system-level integration, production testing, in-field test, diagnosis and repair solutions, cybersecurity, as well as architectures and methods for reliable, safe, and secure operation in the field. The eARTS Workshop wants to offer a forum for industry specialists and academic researchers to present and discuss these challenges and emerging solutions. The workshop's areas of interest include (but are not limited to) the following topics: Automotive Design-for-Test: enable high quality at low cost, Statistical post-processing, Machine Learning, and AI for test and reliability, Latent defect activation during production testing, Built-In Self-Test in automotive systems: digital, analog, mixed-signal, Reuse of test infrastructure and New Product Development acceleration, Dependability challenges of autonomous driving and e-mobility, Functional safety and cyber-security, Automotive standards and certification - ISO 26262, AEC-Q100, Approximate computing for automotive, Verification and validation of automotive systems, Fault tolerance and self-checking circuits, Aging effects on automotive electronics, Power-up, power-down and periodic test, System level test, Functional and structural test generation, Automotive production testing

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## WORKSHOP ON INTELLIGENT METHODS FOR TEST AND RELIABILITY (IMTR'23)

GENERAL CHAIRS : DIRK PFLUEGER (UNIVERSITY OF STUTTGART), MATTHIAS SAUER (ADVANTEST EUROPE) AND MATTEO SONZA REORDA (POLITECNICO DI TORINO)

PROGRAM CHAIRS : HUSSAM AMROUCH (UNIVERSITY OF STUTTGART), KRISHNENDU CHAKRABARTY (DUKE UNIVERSITY), SAID HAMDIOUI (TU DELFT) AND ILIA POLIAN (UNIVERSITY OF STUTTGART)

Room 6

Here you can visit the official website of the workshop: <https://www.gs-imtr.uni-stuttgart.de/imtr23/>

Data collected during different test-related design, manufacturing and operation steps bear huge potential that is heavily under-utilized today. As a consequence, test methods are undergoing a transformation triggered by the advent of next-generation artificial intelligence and data science technology. This workshop aims at bringing the core test community together with interdisciplinary researchers working on various facets of intelligent methods within the test flow. It is underpinned by the Graduate School on Intelligent Methods for Test and Reliability (GS-IMTR) that had been jointly established by Advantest and University of Stuttgart in 2019, to give a major impetus on applied semiconductor test and reliability research. GS-IMTR currently funds ten projects covering the complete test flow, from post-silicon validation and characterization to system-level test and in-field operation. It includes groups working on Computer Science and Electrical Engineering topics ranging from data science and visualization technology to software engineering and radio frequency circuit design. This workshop will leverage the interdisciplinary potentials to consider intelligent methods for test-related problems from the points of view of both: the ETS community and researchers working in different scientific areas



FRIDAY, MAY 26TH, 2023

Workshops 8:30 – 16:00
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## WEBSITE, [cas.polito.it/ETS23](http://cas.polito.it/ETS23)

### Organizing committee

#### General Co-Chair

Daniel Tille (Infineon Technologies)

#### Program Chair

Alberto Bosio (INL - Ecole Central de Lyon)

#### Fringe Workshops Co-Chair

Alessandro Savino (Politecnico di Torino)

#### Publicity Co-Chair

Alexandra Kourfali (ITI Stuttgart, DE)

#### Student Activities Co-Chair

Maria Michael (University of Cyprus)

#### Industry Link Co-Chair

Davide Appello (STMICROELECTRONICS)

#### Awards Co-Chair

Liviu Miclea (CLUJ-NAPOCA University)

#### McCluskey Doctoral Thesis Award Chair

Anne Meixner (Eng.Daughters)

#### Phd Forum Co-Chair

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